JOURNAL OF ALGEBRAIC STATISTICS
Volume 13, No. 3, 2022, p. 4130-4136
https://publishoa.com
ISSN: 1309-3452

FPGA Implementation Of FIR Filter Using Approximate Computing

S. Saravanan M.E.,
Assistant Professor
ECE,K.S.Rangasamy college of Technology,
Namakkal, India
saravanan.s@ksrct.ac.in

Poovarasan R
PG Scholar
ME-VLSI Design K.S.Rangasamy college of Technology,
Namakkal, India
poovarasan29@gmail.com

ABSTRACT

A finite impulse response (FIR) filter is an essential component of any DSP and communication system. The adder and multiplier are two important components of filter architecture. Different adders and multipliers are available in digital circuits, but designing efficient filters requires an efficient adder and multiplier design. To achieve effective computation, the various existing functions of adders are classified, such as the carry select, ripple carry adder, which consumes more area, delay, and power. A novel carry save adder is combined with a structured Wallace tree multiplier and implemented into the digital filter to improve the efficiency of digital design. This novel carry save adder is built with majority logic and implemented in a digital FIR filter. This modified adder and multiplier overcomes the existing drawbacks. It is implemented using Verilog HDL. Compared to other adder techniques, the proposed majority logic produces optimal solutions. This new technique uses less power, has a delay-free carry circuit, and has fewer gate counts.

Keywords— Approximate Adder, FPGA (Field Programmable Gate Array), CSA (Carry Save Adder), Wallace tree Multiplier.

I. INTRODUCTION

A filter is a device or process that removes some unwanted component or feature from a signal. Filtering is a class of signal processing, the defining characteristic of a filter being the complete or partial suppression of some aspect of the signal in the represented synthesis of an arithmetic circuit which is used to verify the digital design by using a logical level method. The existing technique is analyzed using a field-programmable gate array based on signal processing, which is used to improve the efficiency of the individual system. Signal processing faces more challenges in noiseless filter design for effective digital computation. From the reference, the digital FIR filter is designed by using a well-defined adder and multiplier for signal processing applications, but during the signal transmission, this design produces more interference. This paper demonstrates how the area, delay, and power consumption can be brought down for signal processing by utilizing a multiplier and modified conventional carry save adder while keeping up the general signal quality.

II. APPROXIMATE ADDERS

Through splitting the carry propagation chain, estimated adders minimize the critical chain latency and power usage of conventional reliable adder structures, resulting in uncertain additional performance. It rates and contrasts several estimated adders in [6]. The researchers advise an outline of the layout depending on the summation approximation mechanisms, i.e., carrying speculating, segmenting, or estimated adder cell. The cumulative carrying propagation series for every sum of bits is constrained towards previous K bits in this specification. Unless the belief that potential carry propagation for explicit operands is correct, the overall outcome would be entirely accurate. With less likely scenarios of long carry propagation, an incorrect amount of bit can be produced everywhere. The Almost Correct Adder (ACA)'s error behavior could also be counted as Infrequent Broad Magnitude (ILM) errors. The architecture of estimated adders based on segmentation is divided through sub-adders with such a fixed size K that no propagation through segment borders can be transported. Because of this feature, the operands have distinctive bit locations where a carry bit isn't generated. Those adders also cause smaller Errors of magnitude (FSM) whenever segmentation is performed inside the lesser part of the overall output. This approximation class belongs to the Equal Segmentizing Adder (ESA) and Error-Tolerant Adder Form

JOURNAL OF ALGEBRAIC STATISTICS
Volume 13, No. 3, 2022, p. 4130-4136
https://publishoa.com
ISSN: 1309-3452

2 (ETA2). Within the context of the ESA, carry propagation is implemented mainly inside one adder section. In contrast, the element carry feedback in the ETA2 comes from precisely one less important block proceeding it.

III. CARRY SAVE ADDER

A carry save adder is a type of digital adder designed to compute the sum of three or more n-bit binary numbers, and it differs from other digital adders in the way that it results in two outputs, namely sum and carry, which are a sequence of partial sum bits and a sequence of carry bits respectively. Carry save adder is similar to a full adder. When adding two binary numbers, using a half adder followed by a ripple carry adder is faster than using two ripple carry adders. This is because a ripple carry adder cannot compute a sum bit without waiting for the previous carry bit to be produced and therefore has a delay equal to that of n full adders. A carry-save adder, however, makes all of its output values in parallel; for this reason, the total computation time for a carry-save adder is less than ripple carry adders.

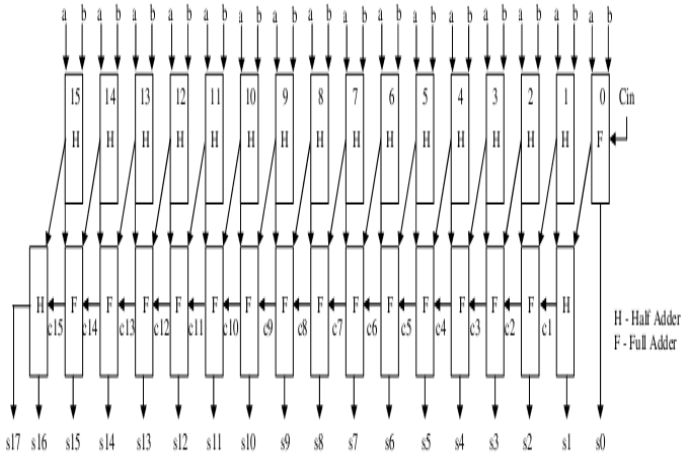

Fig.1 Block diagram for 16-bit Carry Save Adder

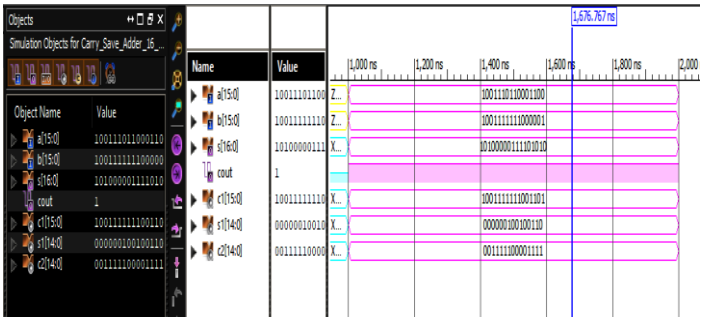

Fig.2 Simulation Result of 16-bit Carry Save Adder

IV. MODIFIED CARRY SAVE ADDER

Approximate The 16-bit conventional CSA [1] shown in fig.1 has 17-half adders (H) and 15-full adders (F). Since, At the last stage, a ripple carry adder is used to generate sum & carry, this structure yields large carry propagation delay. The final stage of CSA is divided into five groups to reduce the delay, as shown in Fig 3. The first group includes n 1+log2 n-bit value, and other groups have log2n-bit value, where n is the bit size of the adder. The divided groups are listed as follows:

JOURNAL OF ALGEBRAIC STATISTICS
Volume 13, No. 3, 2022, p. 4130-4136
https://publishoa.com
ISSN: 1309-3452

1. {c4, s [4:0]}, output s [4:0] is directly assigned as the final output.
2. {c7, x [7:5]} manipulates the partial result by considering c4 is 0.
3. {c10, x [10:8]} manipulates the partial result by considering c7 is 0.
4. {c13, x [13:11]} manipulates the partial result by considering c10 is 0
5. {X [17:14]} manipulates the partial result by considering c13 is0.

Depending on c4 of the first group, the second group mux gives the final result without the carry propagation delay from c4 to c7; depending on c7 of the second group final result, the third group mux gives the final result without the carry propagation delay from c7 to c10; depending on c10 of the third group final result, the fourth group mux gives the final result without the carry propagation delay from c10 to c13 and depending on c13 of the fourth group final result, the fifth group mux gives the final result without the carry propagation delay from c13 to s17. The main benefit of this logic is that each group computes the partial results in parallel and the multiplexers are ready to deliver the final result "instantly" with the minimum mux delay. When the Cin of each group arrives, the final result will be determined "instantly." Therefore, the maximum delay in the carry propagation path is reduced. This same logic has been used for 32 and 64-bit adder structures to achieve higher speeds. The area indicates the design's total cell area, and the total power is the sum of leakage power, internal power, net power, and dynamic power. The proposed result shows that the Modified Carry Save Adder (MCSA) [3] has reduced area and delay and consumes lesser power than CSA.

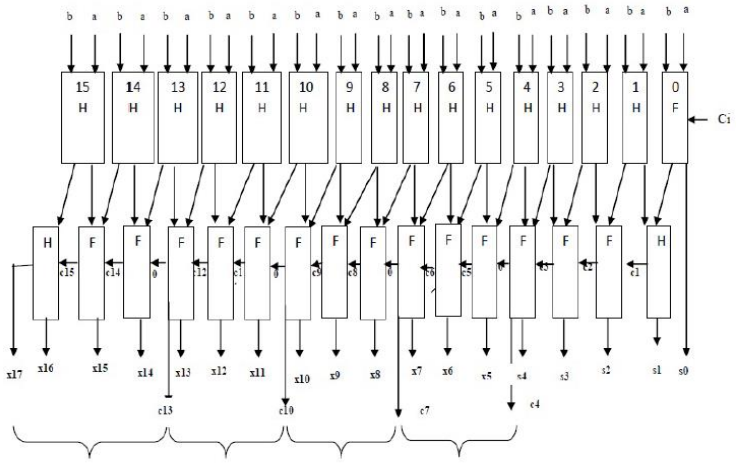

Fig.3 Block diagram of 16-bit Modified Carry Save Adder

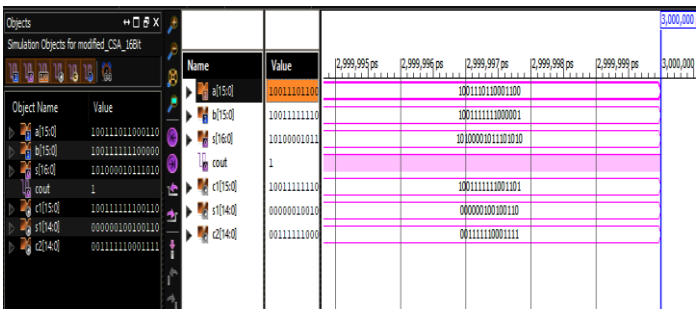

Fig.4 Simulation Result of 16-bit Modified Carry Save Adder

V. PROPOSED MODIFIED CARRY SAVE ADDER

The Proposed Modified Carry Save Adder shown in fig.5 consists of 21 half adders and 11 full adders to deliver the power so minimum than the existing circuit. In carry output, there is a full adder available, the full adder having default input to be '0' (zero), so that a considerable amount of power is utilized by that default input zero value. So we propose a new Modified carry save adder to replace the first full adder of each stage with a half adder. This makes our circuit will consume less power when compared to the existing Modified Carry Save Adder.

JOURNAL OF ALGEBRAIC STATISTICS
Volume 13, No. 3, 2022, p. 4130-4136
https://publishoa.com
ISSN: 1309-3452

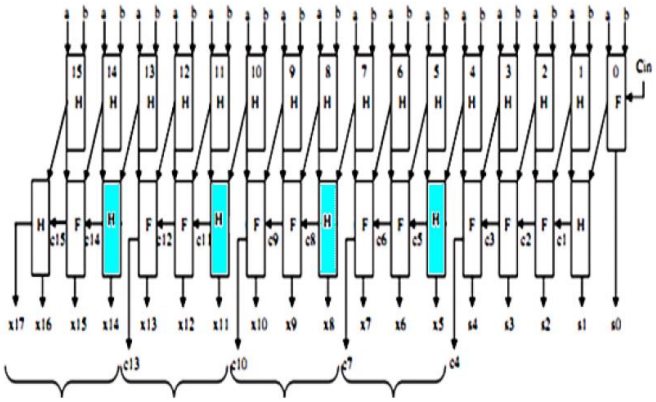

Fig.5 Block diagram of 16-bit Proposed Modified Carry Save Adder

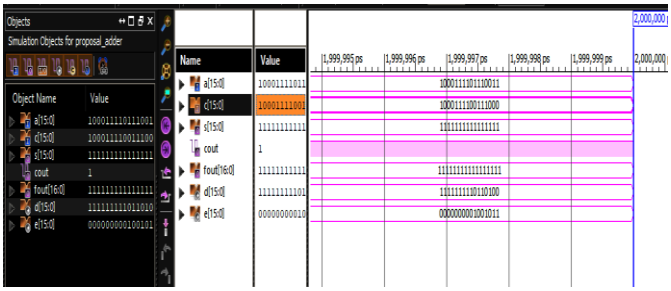

Fig.6 Simulation Result of 16-bit Proposed Modified Carry Save Adder

VI. WALLACE TREE MULTIPLIER

The important design considerations for any chip designer are power consumption, delay, and area. The speed of the circuit changes with the speed/delay of the multiplier; thus, a lot of research has been done to increase the speed of the multiplier so that the delay of the overall circuit can be reduced. The Wallace Tree [12] is a high-speed and area-efficient multiplier, therefore of great importance in high-speed applications. It implements a smooth and efficient hardware technique that multiplies integers using the column compression. Wallace tree [4] gives fast speed because instead of linear dependency as in array multiplier, the total delay is proportional to the logarithm of the word length of the operand of the multiplier.

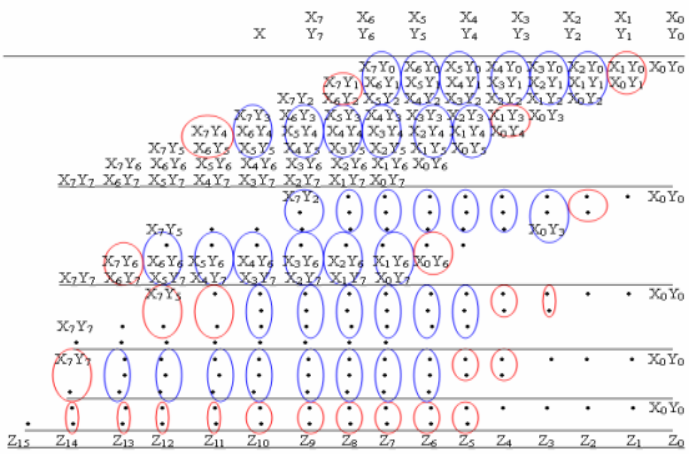

Fig.7 8X8 bit Wallace Tree Multiplier algorithm.

JOURNAL OF ALGEBRAIC STATISTICS
Volume 13, No. 3, 2022, p. 4130-4136
https://publishoa.com
ISSN: 1309-3452

Fig.8 Simulation Result for the conventional 8x8 Wallace Tree multiplier

The Fig.7 shows 8X8 bit multiplication using a reduced complexity algorithm. It can be seen that only X0Y3, X7Y2, X7Y5, and X7Y7 are processed as two bits are very important so that the number stages do not exceed the conventional approach WTM.

VII. FIR FILTER STRUCTURE

Filter design is a major resource for all signal and image processing applications. The overall performance of every individual system is perfectly designed [6] by supporting a digital filter device. The overreaching of the digital processor in the digital world is proposed by using the digital FIR filter based on the ML algorithm; intensified the signals in a digital system is a big challenge for all researchers. The modified carry save & carry-in inversion algorithm has progressively improved the digital FIR filter [3, 4] in the new system design process. The efficiency of existing and new design techniques, which has a simple FIR filter design, fig 9. shows the functional diagram of digital FIR filter design. The performance is evaluated by using the Xilinx ISE simulation tool.

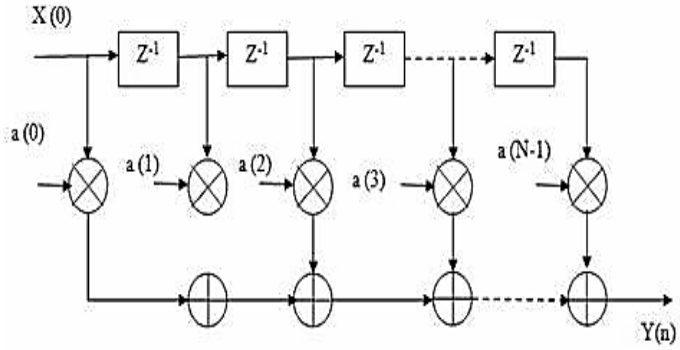

Fig.9 FIR filter structure

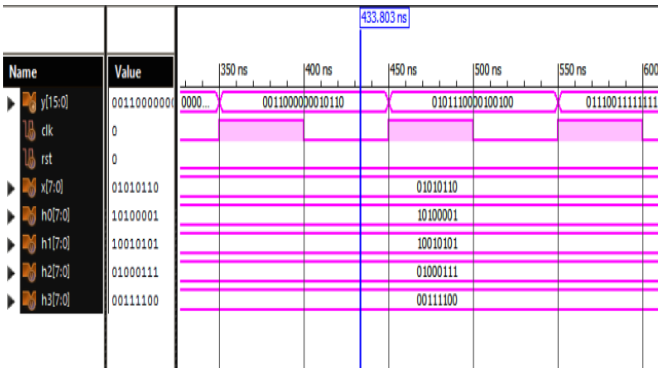

Fig.10 Simulation results of FIR filter.

JOURNAL OF ALGEBRAIC STATISTICS
Volume 13, No. 3, 2022, p. 4130-4136
https://publishoa.com
ISSN: 1309-3452

VIII. RESULT AND DISCUSSIONS

The Digital FIR filter is executed by using Verilog HDL. The DSP design must be enhanced to permit the most effective implementation of these structures as this straightforwardly deciphers into cost and power.

Table 1 Analysis report for FIR filter

Design Block	**No of Slices LUT**	**Delay**
CARRY SAVE ADDER	31	9.221ns
MODIFIED CARRY SAVE ADDER	22	4.706ns
PROPOSED MODIFIED CARRY SAVE ADDER	22	4.706ns
WALLACE TREE MULTIPLIER	91	10.427ns
EXISTING FIR FILTER	384	8.536ns
PROPOSED FIR FILTER	220	2.51ns

The Table .1 compares the proposed method with FIR filter in terms of the number of logic gates and delay usage.

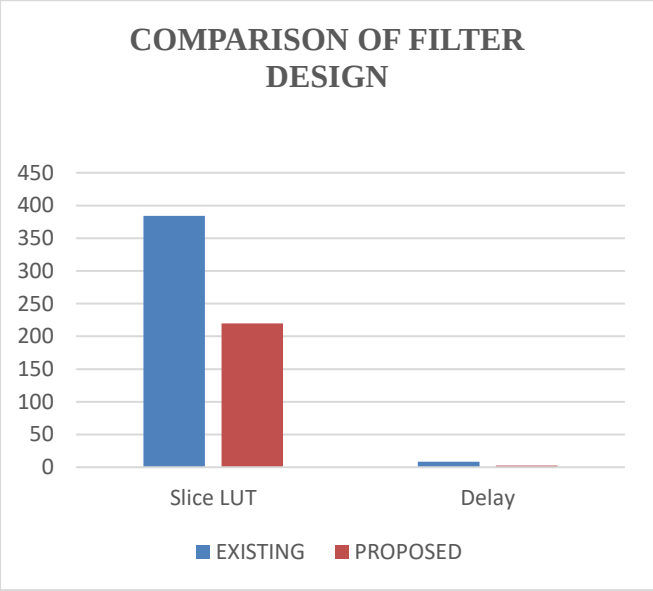

Fig.10.Comparison of FIR Filter Design

IX. CONCLUSION

This paper implemented an FIR filter using the Wallace tree multiplier and proposed a modified carry save adder for area-efficient design. The above techniques are modeled using Verilog and implemented in Xilinx Virtex-5 FPGA. As a result, we can conclude that the proposed architecture achieves better advantages in terms of area, power, and delay when compared to other architectures.

JOURNAL OF ALGEBRAIC STATISTICS
Volume 13, No. 3, 2022, p. 4130-4136
https://publishoa.com
ISSN: 1309-3452

REFERENCES

1. R.Mahalakshmi , Dr.T.Sasilatha., "A power efficient carry save adder and modified carry save adder using CMOS technology," in IEEE International Conference on Computational Intelligence and Computing Research , 2013.
2. Rafiya Banu Nadaf, Dr.UEranna, "An Efficient FIR Filter Design Using Reversible Adder and Multiplier," International Research Journal of Engineering and Technology (IRJET),may 2016.
3. S. Aathilakshmi, R. Vimala, K. R.Aravind Britto, "An Elegance Of A Novel Digital Filter Using Majority Logic For Snr Improvement In Signal Processing", Microelectronics Journal,9 September 2020.
4. V. S. Balaji, Har Narayan Upadhyay, "An implementation of area and power efficient digital FIR filter for hearing aid applications", in Optoelectronics And Advanced Materials – Rapid Communications Vol. 9, No. 5-6, May – June 2015, p. 657 – 662
5. Ms.Monika Gupta, Dr. Sanjeev Sharma, "Design and Implementation of 16-bit Adder using Carry Select and Carry Save Mode", in International Journal of Engineering Trends and Technology (IJETT- Scopus Indexed) – Special Issues - ICT 2020 ISSN: 2231
6. Malothu Rajeswari, Manne Renuka, "Implementation Of Fir Filter Based On Majority Logic Using Approximate Multiplier And Compressor Circuits", Turkish Journal of Physiotherapy and Rehabilitation; 32(2)ISSN 2651-4451 | e-ISSN 2651-446X, Published 2021.
7. S.Soundarya , N.Arumugam, R.Rameshkumar, "Design Of Fir Filter Using EfficientAdder And Multiplier For ECG Signal Processing Applications", International Journal of Engineering Applied Sciences and Technology, 2020.
8. Benisha Bennet; S. Maflin, "Modified energy efficient carry save adder", 2015 International Conference on Circuits, Power and Computing Technologies [ICCPCT-2015]
9. Tahar Bensouici , , AbdelfatahCharef , ImenAssadi, "A new approach for the design of fractional delay by an FIR filter", ISA Transactions Volume 82, November 2018, Pages 73-78
10. Ravikumar A Javali; Ramanath J Nayak; Ashish M Mhetar; Manjunath C Lakkannavar, "Design of high speed carry save adder using carry look-ahead adder", IEEE International Conference on Circuits, Communication, Control and Computing 2014
11. E Jagadeeswara Rao, Jayaram Kumar Kondapalli,T. V. Prasad, "Design of high speed Wallace tree multiplier using 8-2 and 4-2 adder compressors", September 2018International Journal of Engineering & Technology
12. Swati Chulet, Himanshu Joshi, "FIR Filter Designing Using Wallace Multiplier" ,International Journal of Engineering and Technical Research (IJETR)ISSN: 2321-0869, Volume-3, Issue-6, June 2015
13. S.Senthil Sivamanikandan1, J.Jesintha, "Implementation of 8 Bit Dadda Multiplier for Fir Filters by Approximate Compressors", International Journal of Engineering Science and Computing, March 2019
14. N. Udaya Kumar, U. Subbalakshmi, B. Surya Priya, and K. BalaSindhuri, "VLSI Implementation of FIR Filter Using Different Addition and Multiplication Techniques", Zelinka et al. (Eds.): ICSCS 2018, CCIS 837, pp. 483–490, 2018
15. Mahendran Gandhi , M. Periyasamy, S. Murugeswari, S. Praveen Samuel Washburn," A VLSI implementation of FIR filter using self tunable addition and multiplication"
16. Tiago Viegas, "Approximate Computing Techniques for FIR Filters Implementation"